Header separation and reinsertion for 10-Gbit/s variable-length optical packets

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Abstract. We report an all-optical module that performs simultaneous header separation and reinsertion in 10-Gbit/s short optical packets of variable payload length and that consists of two subunits. The first uses a Fabry-Perot filter and an ultrafast nonlinear interferometer (UNI) to perform packet clock recovery. The second is a UNI gate configured as a 2×2 exchange bypass switch that is optically controlled by the recovered clock packets. Using fixed delays, the data packets and the locally generated headers are fed into the 2×2 switch, where header replacement is achieved.
[DOI: 10.1117/1.1872052]

Subject terms: optical packet switching; all-optical clock recovery; exchange-bypass switch; address extraction; optical routing; ultrafast nonlinear interferometer (UNI).

Paper 040337 received Jun. 2, 2004; revised manuscript received Jul. 17, 2004; accepted for publication Sep. 8, 2004; published online Mar. 18, 2005.

1 Introduction

Optical packet switching (OPS) has been proposed as the approach for efficient bandwidth use on the network level, by relieving switching nodes of the electronic bottleneck[1] and by allowing the introduction of intelligent functionalities in the physical layer.[2,3] Effort has also been focused on optical architectures capable of handling asynchronous variable-length packet traffic.[1] However, in order to realize such packet-switched networks, several key functionalities required by a network node, such as optical clock recovery, header processing, buffering, and routing within an optical switching matrix,[4,5] must be performed—ideally in the optical domain. Moreover, the design of OPS nodes and network architecture are still open issues, mainly due to the difficulty of incorporating electronic techniques directly in the optical layer. For example, buffering and data storing are hard to implement in the optical domain, due to the technological immaturity of optical read/write memories. Delay-line-based buffering techniques and architectures are complex to implement and suffer from long access times; moreover, very short or long buffers cannot be implemented using realistic fiber lengths.

Another approach is to design packet-switched networks requiring minimum buffering at each node and to use the optical network itself as buffer. In this scenario, lossless communication can still be achieved, for example, by using the virtual circuit deflection (VCD) protocol[6] and dynamic network traffic management. For instance, if an intermediate link cannot handle the total incoming traffic, an alternative route is selected for part of it. The alternative route may be assigned in a deterministic way, and in this case a new header, known in advance, header must be substituted in the incoming packets. This header, or *tag*, could be a small number of bits containing routing information, processed by the respective tag routers,[7] which have *a priori* information on the traffic status of the network. Such deflection-routed architectures do not require complex optical signal processing or buffering techniques, but require on-the-fly header replacement. Previously reported results[8–10] refer to label-swapping techniques employing electronic header processing, lower-rate headers, and subcarrier multiplexing techniques most suitable for slotted packet-switched networks.

In the present communication we show a simple optical module that can perform on-the-fly header replacement directly in the optical domain. The unit uses two cascaded ultrafast nonlinear interferometric (UNI) gates to perform clock recovery and header separation and reinsertion in short variable-length optical packets. The clock recovery circuit[11] generates packet clocks to optically control a 2×2 exchange bypass switch,[12] which in turn performs header exchange on the 10-Gbit/s incoming data packets. The circuit requires no high-speed electronics and no buffers, and is suitable for deflection-routed optical networks.

2 Experimental Setup

Figure 1 shows the experimental setup with the optical-packet header generator, the clock recovery circuit, and the 2×2 exchange-bypass switch, clearly marked. A distributed feedback (DFB) laser diode, LD1 (1549 nm) was gain-switched at 1.25 GHz to provide 10-ps optical pulses after linear compression The pulse train was modulated with a 2^7-1 PRBS pattern in a $LiNbO_3$ electro-optic modulator (MOD1). The modulated data were then passively rate-multiplied by 8 in a three-stage bit interleaver, in order to produce pseudorandom data patterns at 10 Gbit/s. Two electro-optic modulators, driven by pulse generators, were incorporated at the two outputs of the $\times8$ rate multiplier to generate successive data packets of variable payload length (MOD3) and the new headers (MOD2) to be inserted.

The generated data packets were fed to the clock recovery circuit and the 2×2 exchange-bypass switch by using a

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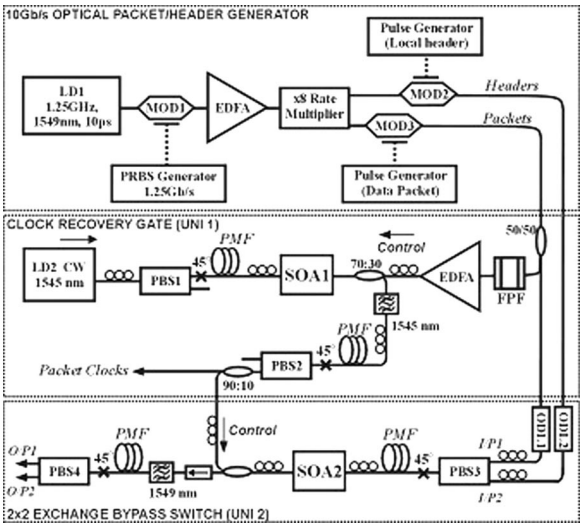

Fig. 1 Experimental setup.

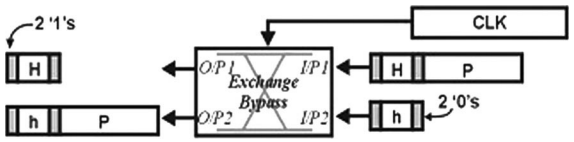

Fig. 2 Bit synchronization requirement.

50:50 fiber coupler. The packet clock recovery circuit[11] consists of a Fabry-Perot filter (FPF) and a UNI gate. The FPF has a free spectral range (FSR) identical to the line rate and a finesse of 20.7. The role of the FPF is to partially fill the zeros in the data sequence by means of spectral filtering and to generate a signal that resembles a packet clock but is amplitude-modulated. This is fed as the control signal to a UNI gate, which is powered by a cw signal generated by a DFB laser diode (LD2) emitting at 1545 nm. Exploiting the nonlinear transfer function of the UNI gate and the saturation properties of the semiconductor optical amplifier (SOA), a packet clock signal with nearly amplitude-equalized pulses is generated.[11] The clock recovery circuit can sustain seven consecutive zeros within the packet, which is due to the low filter finesse used. If a finesse of 80 were to be used, a data sequence with 30 consecutive zeros would still produce packet clocks.

Header separation and reinsertion take place in the 2×2 exchange bypass switch, which is optically controlled by the recovered clock just described. The exchange-bypass switch[12] is a specially configured UNI gate with two input signal ports. Each of the signals in the input ports is analyzed into two orthogonal polarization components via a 45-deg splice located immediately after the input polarization beamsplitter (PBS3). A polarization-maintaining fiber (PMF) is used to birefrigently delay the two orthogonal components of each signal by 50 ps. In the *absence* of a control pulse, the birefrigently delayed signals pass through the SOA, suffering no relative phase change. The polarization of the signals is rotated by 90 deg using a polarization controller (PC), and they travel through another PMF of identical length, thus removing their relative delay and forcing them to recombine in the second 45-deg splice. In this case, the signal entering at port I/P1 appears at O/P1, and the signal entering at I/P2 appears at O/P2. In the *presence* of a control pulse, the polarization component of each signal temporally synchronized with the control pulse experiences a differential phase shift π due to cross-phase modulation (XPM) within the SOA. As a result, the signals recombining at the output now appear exchanged at the output PBS4, that is, I/P1 appears at O/P2, and I/P2 appears at O/P1. The nonlinear switching elements used in the UNI gates were 1.5-nm bulk InGAsP/InP ridge waveguide semiconductor optical amplifiers (SOA1, SOA2) provided by Optospeed S.A., exhibiting small-signal gains of 27- and 25 dB at 1550 nm, and 24 and 22 dB at 1545 nm, respectively, with 80-ps recovery time, when driven with 700-mA current.

Figure 2 shows the necessary synchronization of all three signals to perform on-the-fly header separation and reinsertion on the incoming data packet. Precise temporal synchronization between the three signals is achieved with the optical delay lines ODL1 and ODL2 inserted in the path lines of the packet and new header signals. The packets and the new headers are fed into the 2×2 switch as inputs, I/P1 and I/P2, respectively. The switch is set in its bar state for the duration of the two header sections, so that they pass through the switch, because they are arranged to fall outside the switching window defined by the packet clock. Thus the old header appears in O/P1, and the new in O/P2. When the payload section (P) enters the switch, this is set in its cross state, by arranging for P to fall within the switching window of the packet clock, so that it is transferred to port O/P2 together with the new header. Due to the nonzero rise time of the packet-clock recovery circuit, the packets must contain short guard bands, and this is shown with the gray sections in the figure. In the present experiment the rise time of the packet-clock recovery was 2 bits long, so that the header format contains two logical 1's as guard band at its front to enhance clock extraction, and two logical 0's at its end, to prevent switching with the first two, imperfect clock pulses at the front of the packet clock.

3 Results

The circuit was tested with 10-Gbit/s data packets of short duration and variable payload, header length, and spacing. Figure 3 shows typical results for two packets with durations of 4.4 and 6.6 ns, with 6.4 ns temporal spacing between them. The left-hand column of the figure shows the results for the sequence of the two packets, and the right-hand column shows the results for the 4.4-ns packet in more detail. This packet has a 14-bit header consisting of the sequence 11101100011100 and satisfying the header format requirements for correct operation of the clock recovery circuit. Its payload is 30 bits long and consists of the sequence 00110101011011110101011011010. Figure 3(a) shows the incoming packets with their old headers and payloads, and Fig. 3(b) shows the locally generated headers to be inserted. The new header for the 4.4-ns packet is the sequence 11011011011000. Figure 3(c) displays the recovered clock signals for the packets and shows that they have $1/e$ rise and fall times of 2 and 8 bits respectively, and a maximum amplitude modulation of 1.5 dB. Figure 3(d) shows the packets with their new headers, and Fig. 3(e) the extracted headers. Bit-by-bit checking reveals correct

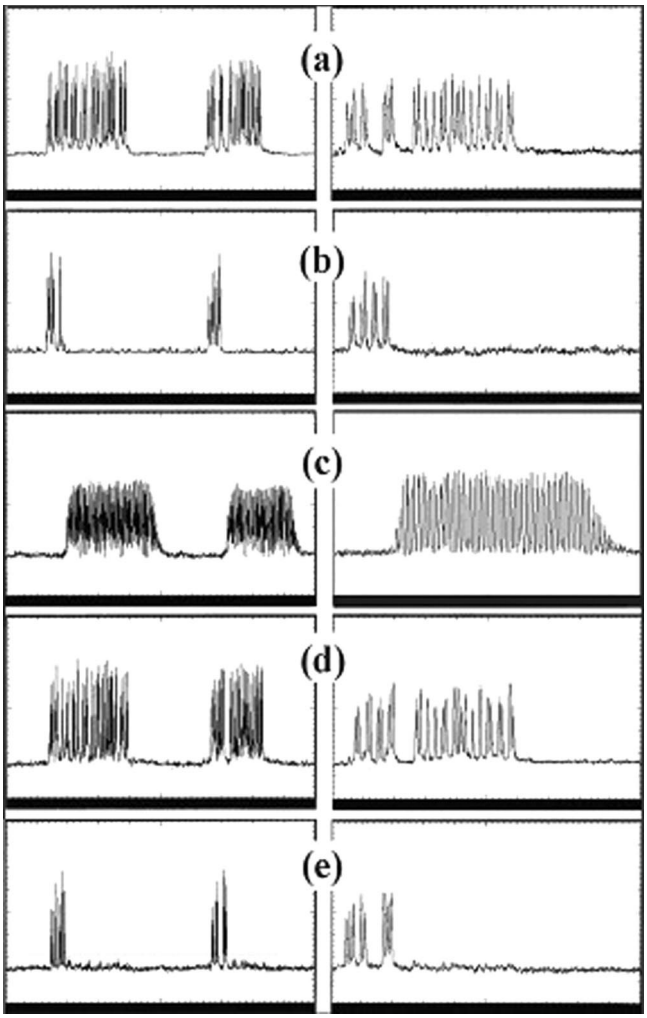

Fig. 3 Pulse traces showing (a) input packets, (b) new headers, (c) recovered packet clocks, (d) packets with new headers, and (e) extracted headers: on the left for 2.5 ns/div, and on the right for 800 ps/div, showing the 4.4-ns packet only.

header replacement and integrity in encoding of the payload at the output of the exchange-bypass switch. The circuit was evaluated with packets of duration between 3 and 20 ns and was found to perform similarly. This is, however, to be expected, because both units of the header separation-reinsertion circuit operate in a bitwise fashion, making it transparent to packet length. The crosstalk at the two output ports of the switch for the cross and bar states was found to be -8 and -10 dB, respectively. The amplitude modulation at the output of the circuit was 1 dB and was identical to that of the original packets, resulting from imperfect rate multiplication in the packet-and-header generator. The clock recovery circuit required 0.8 mW of cw optical power and 100 fJ of control pulse energy. The exchange-bypass switch operated with 4 fJ of energy per pulse for the input signals, and 28 fJ for the control signal. Finally, the excess bandwidth overhead associated with the circuit guardbands was calculated to be 8%. For packet formats with higher payload-to-header ratios, this overhead reduces. For example, in 10 Gbit/s ATM packets the excess overhead reduces to only 2%.

4 Conclusion

We have demonstrated an all-optical network element performing header separation and reinsertion on short, variable-length 10-Gbit/s optical packets. The circuit consists of an optical packet-clock recovery circuit and an optically controlled exchange-bypass switch, both based on nonlinear UNI gates. Given that optical gates have been shown to operate with asynchronous signals,[3] the circuit can be used in asynchronous optical packet-switched networks that employ deflection-routing algorithms to perform header replacement on the fly. The circuit is relatively simple to build, and in principle it should be possible to operate it at higher rates by applying methods for reducing the recovery time of the SOA as reported in Refs. 13 and 14.

Acknowledgment

The authors would like to acknowledge fruitful discussions with Prof. M. Varvarigos of the University of Patras.

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