10 Gb/s BOOLEAN XOR WITH SEMICONDUCTOR OPTICAL AMPLIFIER FIBER SAGNAC GATE

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Abstract : *Boolean XOR logic is demonstrated on a pseudo-data pattern using a semiconductor optical amplifier three-terminal fiber Sagnac gate. Bit pattern switching with low pattern dependence is achieved at 10 Gb/s.*

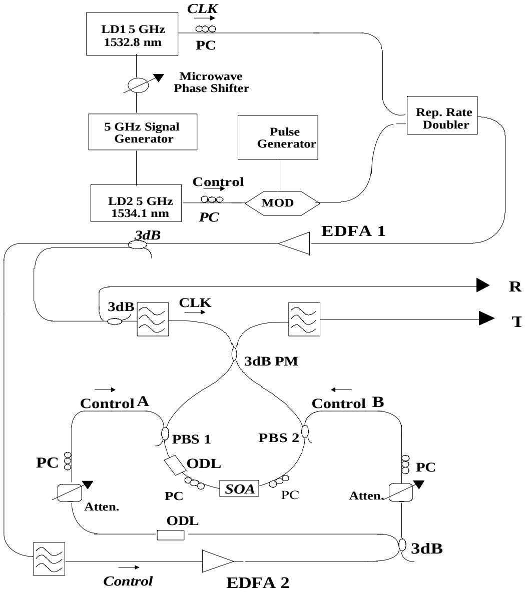
Introduction

The ability to perform high speed, bit serial switching operations has attracted the interest of numerous research groups. The devices that have been mostly studied are based on an optical fiber implementation of the Sagnac interferometer and initially used the nonlinear Kerr effect in optical fibers as the switching nonlinearity /1-3/. With these fiber devices a large number of circuits has been demonstrated including the XOR operation at up to 10 Gb/s /2/. A low switching energy and compact device operating on the same principle but using the nonlinear gain saturation of a semiconductor optical amplifier (SOA) (TOAD/SLALOM) /4-6/ has since been demonstrated. More recently a single arm ultrafast nonlinear interferometer (UNI) has been shown to be capable of logic functionality at up to 100 Gb/s /7/ but without implementing XOR. Lastly, Boolean XOR with a SOA fiber Sagnac gate was demonstrated for full duty cycle pulses at 5 GHz /8/. Boolean XOR is particularly important in decision and comparator circuits as well as for the production of pseudorandom patterns and encryption. In the present communication we report on the pseudo-data pattern XOR operation of a SOA assisted Sagnac interferometer gate at 10 Gb/s with low switching energies and low pattern effect on the switched pulses.

Experiment

In the present experiment the performance of the SOA-assisted Sagnac as an XOR gate was verified using two modulated optical control beams A and B that may take a logical 0 and 1. The logical output is imprinted on a third optical beam (CLK) which is held on input continuously to a logical 1. The experimental configuration is shown in Figure 1.

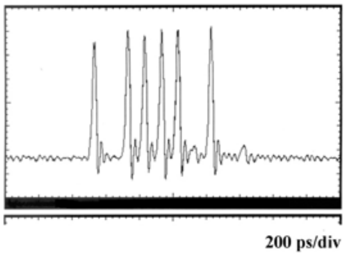
Figure 1: Experimental Setup



The three optical signals were produced from two packaged, fiber pigtailed, gain switched DFB semiconductor diode lasers, LD1 and LD2. The laser diodes were driven from a synthesized RF signal generator at 5 GHz and each produced 12 ps pulses after linear compression with a dispersion compensating fiber of total dispersion - 47.5 ps/nm. The optical clock signal (CLK) was provided by LD1 at 1532.8 nm. The pseudo-data pattern of the two logical control inputs was produced from LD2 at 1534.1 nm using a Li:NbO$_3$ modulator driven from a synchronized, programmable, 500 MHz pulse generator. The repetition frequency of the clock was doubled to 10

GHz with a split, relative delay and combine fiber doubler which introduced a 300 ps relative delay. The doubler also served to construct the final 10 Gb/s, 16 bit-long pseudo-data pattern consisting of 0000101111010000 and shown in Figure 2. The clock and control signals were amplified in a common EDFA 1 and separated with tunable filters before being launched into the gate input ports. The control pulse train was further amplified in EDFA 2 and provided the two control inputs A and B after splitting in a 3dB coupler. Optical power was individually adjusted for A and B with variable attenuators. The SOA assisted Sagnac interferometer gate was constructed using a 3 dB polarization preserving coupler into the ports of which the input-output of the clock signal is injected. Polarization selective fiber couplers (PBS) were used in the loop to couple in and out the orthogonally polarized pulses of the logical control inputs A and B. Polarization controllers (PC) were used in the circuit to define the polarization state of the pulses before entry into polarization sensitive components. The nonlinear interaction between the control and clock pulses was performed in a 1000 μm long, bulk SOA with 100 ps recovery time. Optimum switching was obtained by spatially offsetting the SOA from the center of the loop with a variable optical delay line (ODL) by 30 ps. Precise synchronization between the three optical beams in the SOA was provided with the microwave phase shifter and a variable optical delay line (ODL) in the path of one of the control beams.

Figure 2 : Pseudo-data pattern

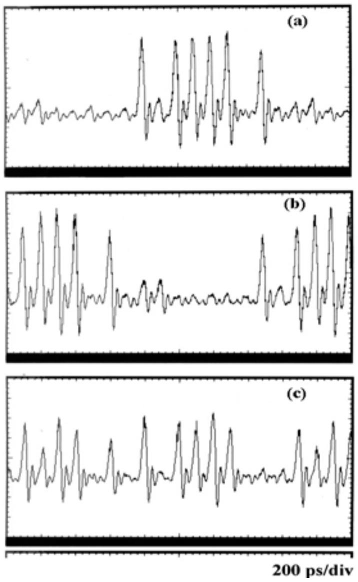


Results and discussion

For successful Boolean XOR between A and B, the transmission port of the gate (T) must record a '1' if either A or B is '1' and a '0' if both A and B are '1'. The output at the T port of the gate was monitored on a 40 GHz sampling oscilloscope and is shown in Figure 3. Figures 3(a) and (b) display respectively the output of the gate for B=0, with any logical A and A=0, with any logical B, that is with either control 'on'. Figures 3(a) and (b) map the time delay between the data patterns entering control inputs A and B. Figure 3(c) shows the output of the gate with both controls A and B present and essentially corresponds to the XOR operation between the pulse trains of Figures 3(a) and (b). Figure 3(c) shows correct operation of the XOR with relatively low pattern effect on the switched out pulses.

During operation the pulse energy for the clock signal was 5 fJ and for the control inputs A and B was 80 fJ and 100 fJ respectively. These energies are indeed low, making the device practical for use with low average power EDFA amplifiers.

Figure 3 : T port outputs; (a) and (b) for single control input for logical A, B=0 and A=0, logical B respectively, (c) for logical A XOR logical B.



Conclusions

We have demonstrated for the first time all-optical Boolean XOR operation on pseudo-data patterns at 10 Gb/s with the three-terminal SOA-assisted Sagnac interferometer gate. Bit pattern switching with low pattern dependence has been achieved with low energies of the incoming clock and data pulses.

Acknowledgments

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