10 Gb/s all-optical boolean XOR with SOA fiber Sagnac gate

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Abstract: All-optical Boolean XOR logic is demonstrated with a three terminal fiber Sagnac interferometer employing a semiconductor optical amplifier. Full duty cycle operation at 10 GHz is shown and low pattern dependence has been achieved on a pseudo-data pattern at 10 Gb/s with low switching energy.

Introduction: Ultra-high speed OTDM multi-access networks are being developed to satisfy the increasing bandwidth demand due to the massive use of Internet and multimedia. Users will access these networks at nodes interfacing the high speed electronics to the ultra-high speed optical data bus by performing on-the-fly a set of all-optical processing operations such as demultiplexing [1], clock recovery [2] and repetition rate reduction [3]. Boolean XOR operation is particular important for OTDM network functions including address and header recognition as well as data encoding and encryption. All-optical Boolean XOR has been demonstrated using the nonlinear fiber loop mirror at 10 Gb/s [4] and more recently at 100 Gb/s [5]. All-optical logic operations have been also performed using the non-linearity of semiconductor optical amplifiers (SOA) [6 - 8] up to 100 Gb/s [9], but so far the demonstration of XOR has been restricted to 1 GHz [10] and more recently to 5 GHz with full duty cycle control signal [11]. Given that semiconductor-based switching devices possess the practical advantages of lower switching energy and lower latency, the demonstration of XOR operation at higher rates is particular important for all – optical applications requiring feedback. In the present communication we report on full duty cycle and pseudo-data control pattern XOR operation of a SOA assisted Sagnac interferometer gate at 10 GHz and 10 Gb/s

respectively with low switching energies and low pattern effect on the switched pulses.

Experiment: The performance of the SOA-assisted Sagnac as an XOR gate was verified experimentally for full duty cycle as well as on a pseudo-data pattern using two optical control beams A and B that may take a logical 0 and 1. The logical output is imprinted on a third optical beam, the clock (CLK), which is held on input continuously to a logical 1. The experimental configuration is shown in Fig. 1. The three optical signals were produced from two packaged, fiber pigtailed, gain switched DFB semiconductor diode lasers, LD1 and LD2. The laser diodes were driven from a synthesized RF signal generator at 5 GHz and each produced 12 ps pulses after linear compression with a dispersion compensating fiber of total dispersion - 47.5 ps/nm. The optical clock signal was provided by LD1 at 1532.8 nm and its repetition rate was subsequently doubled in a split-relative-delay-and-recombine fiber doubler. The pseudo-data pattern of the two logical control inputs was produced from LD2 at 1534.1 nm using a Li:NbO_3 modulator driven from a synchronized, programmable, 500 MHz pulse generator. The doubler also served to construct the final 10 Gb/s, 16 bit-long pseudo-data pattern consisting of 0000101111010000. The clock and control signals were amplified in a common EDFA 1 and separated with tunable filters before being launched into the gate input ports. The control pulse train was further amplified in EDFA 2 and provided the two control inputs A and B after splitting in a 3 dB coupler. Optical power was individually adjusted for A and B with variable attenuators. The SOA-assisted Sagnac interferometer gate was constructed using a 3 dB polarization preserving coupler which was used for clock signal insertion and extraction. Polarization selective fiber couplers (PBS) were used in the loop to couple in and out the

orthogonally polarized pulses of the logical control inputs A and B. Polarization controllers (PC) were also employed in the circuit to define the polarization state of the pulses before entry into polarization sensitive components. The nonlinear interaction between the control and clock pulses was performed in a 1000 μm long, bulk SOA with 100 ps recovery time. Optimum switching was obtained by spatially offsetting the SOA from the center of the loop by 30 ps, using a variable optical delay line (ODL). The three optical beams were precisely synchronized in the SOA with a microwave phase shifter and a variable optical delay line (ODL) located in the path of one of the control beams.

Results and Discussion: For successful Boolean XOR between A and B, the transmission port of the gate (T) must record a '1' if either A or B is '1' and a '0' if both A and B are '1'. The output at the transmission port of the gate was monitored on a 40 GHz sampling oscilloscope with a 30 GHz detector. Figs. 2 (a) and (b) illustrate the logic output of the gate with full duty cycle and with data modulated control beams, respectively, for the four logical combinations of controls A and B and prove correct XOR operation for either cases. In particular Fig. 2 (b) shows that XOR is successfully confirmed bit by bit between the mapped to the clock time delayed data patterns A and B with relatively low pattern effect on the switched out pulses. The contrast ratio between the ON-OFF states of the gate was as high as 14 : 1 and 12 : 1 and was achieved with switching energy up to 50 fJ and 100 fJ for full duty cycle and pseudo-data pattern operation respectively. Note that these energies are low for both cases despite the simultaneous presence of the two control beams that deeply saturate the SOA making the device practical for use with low average power EDFAs. The performance of the gate in terms of the switching energy and the

contrast ratio depends on the gain and the recovery time of the SOA as well as on the width of the control and signal pulses. Of these parameters, the most easily adjusted experimentally are the widths of the optical pulses, which will also be crucial in defining the highest operating rate of the SOA-assisted gate. In order to assess whether the 12 ps pulses used in the present experiment were appropriate, the temporal window within which the gate switches was measured by delaying control A with respect to the clock while monitoring the transmission port of the gate. The resulting switching window is shown in Fig. 3 indicating that the ON state of the gate is obtained over approximately 15 ps. As this is short compared to the 12 ps pulses, it is expected that the use of shorter pulses will improve the contrast ratio of the gate and will certainly be necessary for higher rate operation of the device.

Conclusions: We have demonstrated all-optical Boolean XOR logic for full duty cycle operation at 10 GHz and with pseudo-data patterns at 10 Gb/s using a SOA-assisted fiber Sagnac interferometer. This has been achieved with low energies of the incoming clock and data pulses, low pattern effect and adequate contrast ratios for optical logic applications. The XOR demonstration is particular important for future ultrafast OTDM networks since it opens the possibility for the implementation of other more complicated all-optical circuits that require the simultaneous presence of two control beams.

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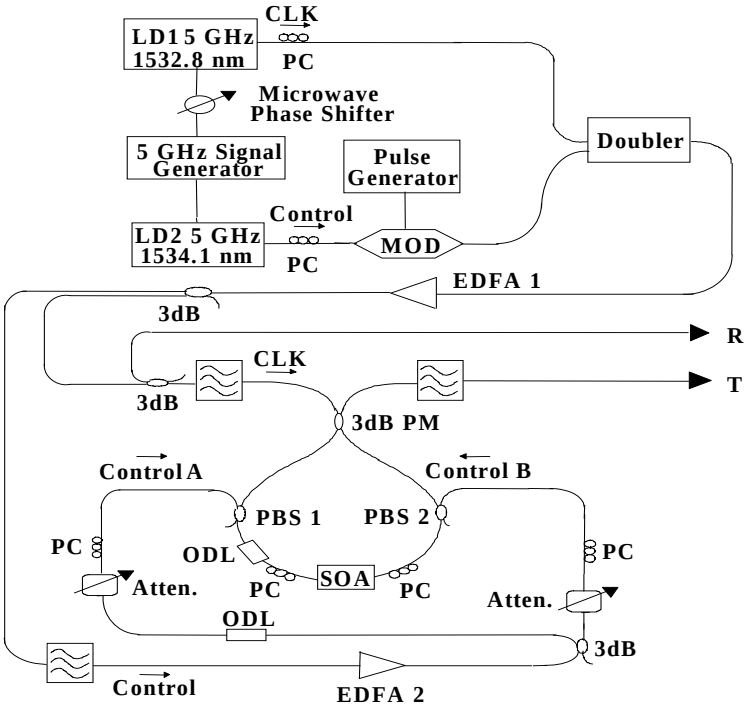
Captions

Figure 1 Experimental setup

Figure 2 Logic output at transmission port of the gate at 10 GHz (a) and 10 Gb/s (b) for the four logical combinations of controls A and B

Figure 3 Switching window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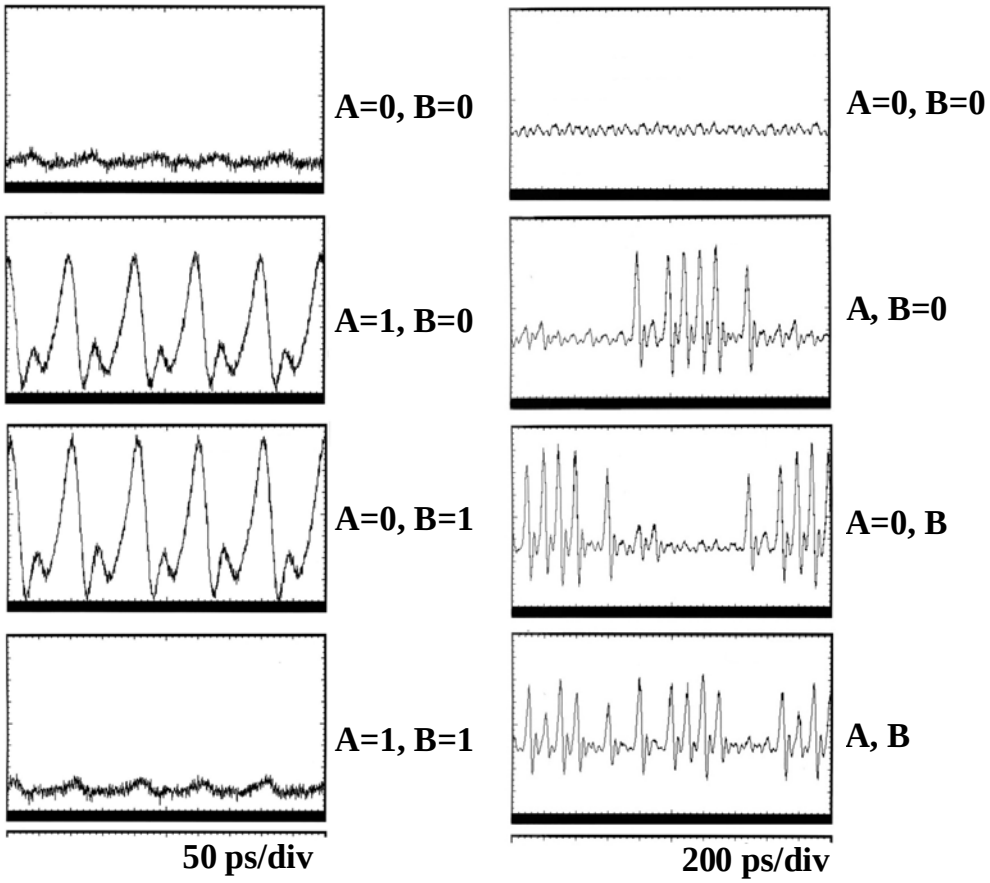
LD1 5 GHz
1532.8 nm
PC
Microwave
Phase Shifter
Doubler
5 GHz Signal
Generator
Pulse
Generator
Control
LD2 5 GHz
1534.1 nm
PC
MOD
EDFA 1
3dB
R
CLK
T
3dB
3dB PM
Control A
Control B
PBS 1
PBS 2
PC
ODL
PC
SOA
PC
PC
Atten.
Atten.
ODL
3dB
Control
EDFA 2


A=0, B=0
A=1, B=0
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A=1, B=1
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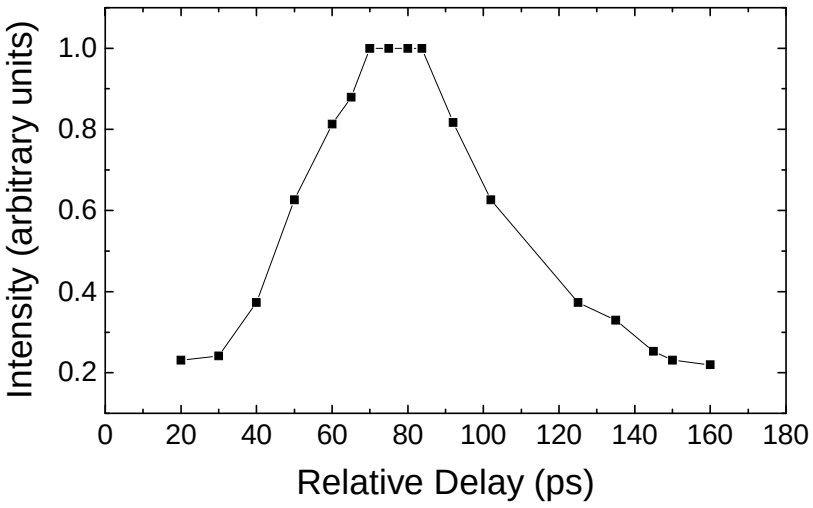
A=0, B=0
A, B=0
A=0, B
A, B
200 ps/div


Intensity (arbitrary units)
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0.6
0.4
0.2
0
20
40
60
80
100
120
140
160
180
Relative Delay (ps)